09/488,865

REMARKS

Claims 23-42 are all the claims pending in the application. Previous claims 1-7 stood rejected and prior art grounds. The cancellation of claims 1-7 renders this rejection moot; however, below is a discussion of the applied reference with respect to the presently claimed invention to illustrate the non-inapplicability of the applied references to the claimed invention.

I. The Prior Art Rejections

Claims 1-7 stood rejected under 35 U.S.C. §103(a) as being unpatentable over Barr (U.S. Patent No. 5,758,056) in view of Shingai (U.S. Patent No. 5,293,612). More specifically, the Office Action states that Barr discloses a memory system having address identification, comprising: determining means for determining addresses of defective memory locations. (see abstract and col. 3, lines 50-52). The Office Action admits that Barr does not disclose a means for determining a physical location of the defective address. However, the Office Action asserts that Shingai discloses a means for translating or determining virtual address into physical address by using a look"up table, (see col. 3, lines 14-16). Therefore, the Office Action concludes that it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teaching of Shingai into the invention of Barr to produce a physical address location of the defected address to correct errors.

Barr discloses a memory system which restores full functionality to a dynamic random access main memory having at least one defective bit. In Barr, the memory system is integrated on an industry standard memory module which is plugged into a host computer system. The memory module incorporates a block of DRAM main memory, an SRAM replacement memory, a non-volatile memory which stores a map of defective memory locations within the main memory, and a process control module (PCM) operable in multiple modes, which manages a defective address identification and replacement process. The PCM, which contains high-speed registers, in addition to decoding and control logic, and is implemented as a high-speed application-specific integrated circuit (ASIC). The PCM, which is coupled to both the host system memory address and data buses, recognizes addresses of defective memory locations within the main memory block and, in response to such recognition, suppresses output from the main memory block and provides a replacement address within the high-speed SRAM memory. The data stored at the replacement address is output to the system data bus. The process operates with sufficient speed to ensure that there is no degradation in main memory access time. The non-volatile memory can be updated by the host system to correct newly discovered defects in the main memory without removing the memory module from the system.

Shingai discloses a method and process for providing a memory dump of less than the entire contents of memory. In Shingai, the memory locations to be dumped are selected on the basis of recency of use, so that there is a high probability that portions of memory needed for analysis or evaluation of the computer system will be included in the selective dump. Preferably, the selection is made on the basis of information or hardware which is already provided in the

computer system. In Shingai, memory to be dumped is selected on the basis of memory locations encoded for by a translation lookaside buffer.

To the contrary, with the claimed invention, a device under test (e.g., memory device) is tested for defects and a two-dimensional failmap is produced on a real time display. In order to identify the electrical location of a given defective element of the device under test, the two-dimensional coordinate of the failmap must be translated into an n-dimensional logical location (e.g., word-line, bit-line, DQ, etc.). More specifically, as defined by independent claim 23, the invention includes "applying a set of displacement and mirror factors to said physical cell coordinate to translate said physical cell coordinate into a logical address."

Conventionally, a programmer would prepare an algorithm or look up table relating to the entire device under test to perform the address translation. However, with the invention, the user (without the aid of a programmer) only needs to prepare a lookup table relating to the smallest repeatable unit of the device under test. Independent claims 30 and 37 define "preparing a look up table for translating physical cell coordinates of said repeatable memory cells into logical addresses." In addition, the user supplies coefficients relating to linear operation on the lookup table values and horizontal and vertical mirroring and displacement from the reference block (as well as any additional required features) and the invention applies the look up table to all other smallest repeatable units to perform the address translation for the entire device under test. Also, the recursive nature of the invention requires substantially reduced input from the user by defining larger and larger repeatable units.

Thus, with the invention, only sets of 6 coefficients and a look up table and the recursive partitioning information are required from the user and the assistance, design time, debugging time and other costs associated with conventional customized address translation programs are avoided.

Barr and Shingai are completely unrelated to the invention because they relate to (hardware) detection methods of locating defective memories. To the contrary, the claimed invention translates any physical cell coordinate (x, y) location (not just failed locations) to a logical, electrical, or structural address. Therefore, neither applied reference teaches or suggests the invention as defined by the claims. Therefore, Applicants respectfully submit that the application as defined by the present claims is patentable and that the application is in condition for allowance.

II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 23-42, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 12/13/02

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Marked Up Version of Changes Made:

IN THE TITLE:

Please change the title throughout METHOD FOR TRANSLATING [TWO-DIMENSIONAL] PHYSICAL CELL-COORDINATES OF A MEMORY PRODUCT TO N-DIMENSIONAL [PHYSICAL] ADDRESSES.

Please cancel claims 1-22 without prejudice or disclaimer.

Please add the following new claims:

23. A method for translating physical memory cell coordinates of a memory device, said method comprising:

inputting a physical cell coordinate of a memory device; and

applying a set of displacement and mirror factors to said physical cell coordinate to translate said physical cell coordinate into a logical address.

24. The method in claim 23, wherein said logical address comprises an N- dimensional logical address, wherein N comprises a natural number.

25. The method in claim 23, further comprising:

identifying repeatable memory cells of said memory device;

preparing a look up table for translating buffer coordinates of a reference memory cell of said repeatable memory cells;

displacing information from said look up table to correspond to said repeatable memory cells; and

modifying results of said displacing by a linear operation.

26. The method in claim 25, wherein said displacing includes mirroring said information from said look up table to correspond to said repeatable memory cells.

27. The method in claim 25, wherein said reference memory cell comprises a smallest repeatable memory cell.

28. The method in claim 27, further comprising:

identifying a first level of repeatable memory cells, having a size larger than said smallest repeatable memory cell;

identifying a second level of repeatable memory cells, having a size larger than said first level of repeatable memory cells; and

recursively displacing said information from said look up table to correspond respectively to said smallest repeatable memory cells, said first level of repeatable memory cells, and second level of repeatable memory cells.

29. The method in claim 25, wherein said displacing and modifying comprise translating said buffer coordinates using the following function:

$$g(x,y) = A \bullet f(ax + b, cy+d) + B;$$

wherein variable A comprises one of an amplification and pattern reversal value, variable B comprises a linear displacement of said information from said look up table, variable b comprises a horizontal displacement from said reference memory cell, variable d comprises a vertical displacement from said reference memory cell, variable a comprises horizontal mirroring and variable c comprises vertical mirroring.

30. A method for translating physical memory cell coordinates of a memory device to logical addresses, said method comprising:

identifying repeatable memory cells of said memory device;

preparing a look up table for translating physical cell coordinates of said repeatable memory cells into logical addresses; and

displacing information from said look up table to correspond to said repeatable memory cells.

31. The method in claim 30, wherein said logical addresses comprise N-dimensional logical addresses, wherein N comprises a natural number.

32. The method in claim 30, further comprising modifying results of said displacing by a linear operation.

33. The method in claim 30, wherein said displacing includes mirroring said information from said look up table to correspond to said repeatable memory cells.

34. The method in claim 30, wherein said reference memory cell comprises a smallest repeatable memory cell.

35. The method in claim 34, further comprising:

identifying a first level of repeatable memory cells, having a size larger than said smallest repeatable memory cell;

identifying a second level of repeatable memory cells, having a size larger than said first

level of repeatable memory cells; and

recursively displacing said information from said look up table to correspond respectively to said smallest repeatable memory cells, said first level of repeatable memory cells, and second level of repeatable memory cells.

36. The method in claim 30, wherein said displacing comprise translating said buffer coordinates using the following function:

$$g(x,y) = A \bullet f(ax + b, cy+d) + B;$$

wherein variable A comprises one of an amplification and pattern reversal value, variable B comprises a linear displacement of said information from said look up table, variable b comprises a horizontal displacement from said reference memory cell, variable d comprises a vertical displacement from said reference memory cell, variable a comprises horizontal mirroring and variable c comprises vertical mirroring.

37. A method for translating physical memory cell coordinates of a memory device to logical addresses, said method comprising:

identifying repeatable memory cells of said memory device;

identifying a first level of said repeatable memory cells, said first level having a size larger than a smallest repeatable memory cell;

identifying a second level of said repeatable memory cells, said second level having a size larger than said first level of repeatable memory cells;

preparing a look up table for translating physical cell coordinates of said repeatable memory cells into logical addresses; and

recursively displacing said information from said look up table to correspond respectively to said smallest repeatable memory cells, said first level of repeatable memory cells, and second level of repeatable memory cells.

38. The method in claim 37, wherein said logical addresses comprises N-dimensional logical addresses, wherein N comprises a natural number.

39. The method in claim 37, further comprising modifying results of said displacing by a linear operation.

40. The method in claim 37, wherein said displacing includes mirroring said information from said look up table to correspond to said repeatable memory cells.

41. The method in claim 37, wherein said displacing comprise translating said buffer coordinates using the following function:

$$g(x,y) = A \bullet f(ax + b, cy+d) + B;$$

wherein variable A comprises one of an amplification and pattern reversal value, variable B comprises a linear displacement of said information from said look up table, variable b comprises a horizontal displacement from said reference memory cell, variable d comprises a vertical displacement from said reference memory cell, variable a comprises horizontal mirroring and variable c comprises vertical mirroring.

42. A method for translating physical memory cell coordinates of a memory device, said method comprising:

inputting a physical cell coordinate of a memory device; and

applying a set of displacement and mirror factors to said physical cell coordinate to translate said physical cell coordinate into one of a logical address, an electrical address, and a structural address,

wherein said logical address, said electrical address, and said structural address comprise N-dimensional addresses, wherein N comprises a natural number.